# DEPARTMRNT OF ELECTRICAL ENGINEERING GOVT. POLYTECHNIC,BHADRAK 



## LECTURENOTES

## ANAEOG ELECTRONICS \& OPAMP

## SEMESTER-4 ${ }^{\text {TH }}$ <br> Prepared <br> by

TAPAN KUMAR DAS
Lecturer in Electronics \& Telecommunication

## CONTENTS

| S.No | Chapter Name | Page No |
| :---: | :--- | :---: |
| 1 | PN-Junction | $3-8$ |
| 2 | Rectifier | $9-13$ |
| 3 | Filter | $14-16$ |
| 4 | Bipolar Junction Transistor | $17-30$ |
| 5 | Transistor Biasing | $31-34$ |
| 6 | Feedback Amplifier | $35-38$ |
| 7 | Multistage Amplifier | $39-44$ |
| 8 | Reference | 45 |

## CHAPTER-I

## PN-JUNCTION

## PN-JUNCTION:

$>$ When a p-type \& n-type material are suitably joined the contact region is called pe-funetion.
$>\mathrm{PN}$-junction is very important for manufacturing different electronic devices hike rectifier,LED, Zener diode.
> Structure:

(b)
(c)


Cathode

Schematic symbol

## PROPERTIES OF PN-JUNCTION

Stripe marks cathode
$>$ The p-type material has majority holes \& minority free electrons .Each hole is
associatedby a -ve ion. Similarly the n-type material has majority free electrons \& minority holes.
Each free electrons is associated by +ve ion.
> When this p -type \& n-type material are joined to form pn-junction, at the junction the $\quad$ +vehole on p -side \& the -ve free electron on n -side attract each other \& cancel after combination.Due to this combination a net -ve charge develops on $p$ side \& net + ve charge
$>$ The region across which barrier potential exist is called depletion layer, because this layeris depleted of charge carrier.

## WORKING PRINCIPLE OF PN JUNCTION :

* For proper operation of pn-junction an external supply should be used. The external supply magnitude should be greater than barrier potential \& applied in forward condition i.e. +ve terminal is connected to p-type \& -ve to n-type as shown in figure below :

*If there is no external voltage applied across the pn-junction, a barrier potential exists across the junction \& due to this the pn-junction is not conducting \& current through pn-junction is zero.
*When external voltage is applied, the majority holes in p-type are repelled by the +ve terminal of the source \& free electrons in n-type are repelled by the -ve terminal of the sources As an result both free electrons \& holes move towards the junction \& cancels barrier potential. This movement produces current flow through the pn-junction.
*It is clear from the figure that current flow inside the pn-junction is due to two types of charge carrier, i.e. free electrons \& holes, but outside the junction current is due to only free electrons.


## BIASING OF PN JUNCTION :

[^0]a) Zero bias
b) Forward bias
c) Reverse bias

Zero Bias: The pn-junction without any external supply is called zero bias. Under this condition the pn-junction is not conducting due to existence of barrier potential.

## Forward Bias

$>$ If p-type material is connected to +ve \& n-type to -ve of external supply, yhe pnjunction issaid to be forward bias.
> FIGURE:

$>$ Due to forward biasing the +ve terminal of external supply repels the holes towards the junction Similarly the majority free electrons in n-region repelled by the -ve terminal of thesupply. As a result there is a continuous movement of free electrons \& holes across the junction. The pn-junction is now conducting.
tt is clear from the figure that current inside the pn-junction is due to two types of chargecarriers, that is free electrons \& holes, but out side the junction current is due to only free electrons.

Due to forward biasing the barrier potential is eliminated. Depletion width decreases.
Due to forward biasing resistance of pn-junction decreases \& conductivity increases.

## Reverse Biasing

$>$ When p-type is connected to -ve \& n-type to +ve of external supply the pn-junction is saidto be reverse biased.
> Figure:

$>$ Under reverse biased condition the majority holes of p-type are attracted by -ve terminal ofthe supply \& majority free electrons ofn-type are attracted by +ve terminal of supply. As a result the majorit free electrons \& holes are moving away from the junction. No majority carrierscross the junction. The PN-junction is said to not conducting \& no current flow threagh the pn-junction.
$>$ Due to minority carrier very small current, in the range of micro ampere flows across thepn-junction. This small minority current sometimes assumed as approximately zero.
> Due to reverse biasing the resistance of pn-junction increases \& conductivity decreases tovery smallyalue.
$>$ Due to reverse biasing depletion width increases. The barrier potential actsin the same direction as the external supply. Hence it can not be cancelled.

## V~I CHARACTERISTIC OF PN-JUNCTION :

The graph which shows the relation between voltage applied across a pn-junction \& currentflowing through it is called $\mathrm{V} \sim \mathrm{I}$ characteristic.
$>$ Two types of $\mathrm{V} \sim \mathrm{I}$ characteristic :
a) Forward V $\sim I$ characteristic
b) Reverse V~I characteristic

## Forward V~I Characteristic :

> The characteristic under forward bias condition of pn-junction is called forwardcharacteristic.
$>$ By changing the position of variable resistor R number of readings are taken from voltmeter\& ammeter. All readings are plotted on a graph paper \& the resulting graph is called forward V~I characteristic.
$>$ Graph:


When the voltage across the pn-junction is zero, no current flows. If we increase the voltageacross pn-junction in forward direction, at first current increases very slowly with voltage, but after certain voltage, current increases very rapidly with voltage. This voltage is called Knee voltage.
$>$ Below Knee voltage current is very small due to barrier potential, because supply voltage istrying to cancel the barrier potential. But after knee voltage, barrier potential completely cancelled \& current rises very rapidly.

## REVERSE CHARACTERISTIC:

$>$ The characteristic under reverse condition of pn -junction is called reverse characteristic.
$>$ The characteristic can be drawn by taking readings for different position of variable resistor.
$>$ If the voltage increases from zero to onwards in -ve direction, at first current rises veryslowly with voltage. This process continues upto a certain voltage known as avalanche breakdown voltage VB.
> At VB current suddenly increases to a very high value.
> Above break down voltage if voltage across pn-junction increases further, then it has noeffectover the current .

At break down voltage the pn-junction may burnt due to excess heat.

## Complete V~I Characteristic:



## CHAPTER-2

## RECTIFIER

## RECTIFIER:

The electronic device which converts AC to DC is called rectifier.

## TYPES OF RECTIFIER:

1.Half wave rectifier
2. Full wave rectifier:
a) Center tapped full wave rectifier
b) Bridge type full wave rectifier

## HALF WAVE RECTIFIER:

*The rectifier which rectifies only one half cycle of ac I/P supplys called half wave rectifier.
*Circuit Diagram:


## Circuit details:

It consists of a step down transformer T , diode D , load resister $\mathrm{R}_{\mathrm{L}}$. The transformer is used to transfer the input ac supply from primary to secondary in step down mode. Diode D used for rectification. The dc output develops across load resistor $\mathrm{R}_{\mathrm{L}}$.

## OPERATION:

1. During the +ve half cycle of ac input, terminal A is $+\mathrm{ve} \& \mathrm{~B}$ is -ve . This makes diode D forward biased. Hence the diode acts as a closed switch.Now current flows through the secondary circuit \& also through load resistor RL.
2. During the -ve half cycle of ac input supply, terminal A is -ve \& B is +ve . This makes diode D reverse biased \& acts as an open switch. Due to open path, no current flows through the secondary circuit. Hence no output voltage.
3. It is clear from the above that current through RL always flows in one direction, i.e. only during the +ve half cycle. This provides one direction $\mathrm{o} / \mathrm{p}$ voltage. This $\mathrm{o} / \mathrm{p}$ is dc.
4. I/P \& O/P wave form:


## DISADVANTAGES:

1-It contains more ripple.Hence requirs elaborate filtering.
2-Output power is low,because a.c. supply delivers ;power only half the time.

## CENTER-TAPPED FULL WAVE RECTIFIER

It is one type of full wave rectifier, which rectifies both half cycle of ac I/P supply.

## Circuit Diagram:



## Circuit Detail:

It consists of a center tapped transformer T, two diodes $\mathrm{D}_{1} \& \mathrm{D}_{2}$, load resistor RL. The transformer T transfers the ac input from primer to secondary in step down mode. Diodes $D_{1} \& D_{2}$ used for rectification. The dc output develops across load resistor $\mathrm{R}_{\mathrm{L}}$.

## Operation:

1. During the +ve half cycle of ac I/P supply, the terminal A is $+\mathrm{ve} \& \mathrm{~B}$ is -v . This makes diode D1 forward biased \& diode D2 reverse biased. Hence D1acts as a closed switch \& D2 as open switch. Due to open switch, no current flows through the lower portion of the secondary circuit. Current only flowfonly through the upper portion of secondary circuit as shown by solid arrow.
2. During the -ve half cycle of ac input supply terminal A is - ve $\&$ terminal B is + ve. This makes diode D1 reverse biased \& diode D2 forward biased. Hence D1 acts as open switch \& D2 as closed switch. No current flows through the upper portion of secondary circuit. Current flows only throughthe hower portion as shown by dotted arrow.
3. It is clear from the above that for both half cycle of ac input, current through Rbflows in same direction i.e. from D to C . This current is dc.

## ADVANTAGES:

1-requirs only two diodes.
2-It not requirs elaborate filtering.

## DISADVANTAGES:

1-It uses centertapped transformer \&It is difficult to locate perfect centertapped on the secondary.
2-The dc output is small as each diode utilises only one half of the transformer secondary voltage. 3-Requirs high PIV diodes.

## BRIDGE RECTIFIER:

It is one type of full wave rectifier which rectifies beth half cycle of ac input supply.

## Circuit Diagram :



## Operation:

1. During the +ve half cycle of ac $\mathrm{i} / \mathrm{p}$ supply terminal A is $+\mathrm{ve} \&$ terminal B is -ve . This makes diode D1 \& D3 forward biased \& D2, D4 reverse biased. Hence D1, D3 acts as closed switch but D2, D4 acts as open switch. Current flows through the secondary circuit as shown by solid arrow.
2. During the -ve half cycle of ac input supply, terminal A is -ve \& terminal B is +ve. This makes diode D1 \& D3 reverse biased \& D2,D4 forward biased. Hence D1, D3 acts as open switch \& D2, D4 closed switch. Current flows through the secondary circuit as shown by dotted arrow.
3. It is clear that for both half cycle of ac $\mathrm{i} / \mathrm{p}$, current through RL flows in same direction i.e. from C to D . This is dc output.

## ADVANTAGES:

1-No need of centertapped transformer.
2-Output is twice that of centertapped circuit for same secondary voltage.
3-The PIV is one half of the center-tap circuit.

## DISADVANTAGES:

1-It requirs four diodes.
2-Not suitable for small secondary voltage.

## AVERAGE /DC VOLTAGE \& CURRENT OF RECTIFIER:

*FOR HALF WAVE RECTIFIER:

$$
\begin{aligned}
& \mathrm{I}_{\mathrm{dc}} / \mathrm{I}_{\mathrm{av}}=\mathrm{Im} / \pi \\
& \mathrm{V}_{\mathrm{dc}} / \mathrm{Vav}=\mathrm{V}_{\mathrm{m}} / \pi
\end{aligned}
$$

*FOR FULL WAVE RECTIFIER:
$\mathrm{I}_{\mathrm{dd}} / \mathrm{I}_{\mathrm{av}}=2 \mathrm{Im} / \pi$ $\mathrm{Vdc} / \mathrm{Vav}=2 \mathrm{Vm} / \mathrm{pi}$

## RECTIFIER EFFICIENCY:

It is the ratio of dc output power to ac input powera rectifier.
Mathematically given by :
In percentage

$$
\begin{aligned}
& \eta=\mathrm{P}_{\mathrm{dc}} / \mathrm{P}_{\mathrm{ac}} \\
& \eta=\left(\mathrm{P}_{\mathrm{dc}} / \mathrm{Pac} \mathrm{a}\right) \times 100
\end{aligned}
$$

Where
$\mathrm{P}_{\mathrm{dc}}=\mathrm{DC} \mathrm{O} / \mathrm{P}$ power
$\mathrm{P}_{\mathrm{ac}}=\mathrm{AC} \mathrm{O} / \mathrm{P}$ power

## RECTIFIER EFFICIENCY OEHALF WAVE RECTIFIER:

We know for half wave rectifer

$$
\begin{aligned}
& \mathrm{I}_{\mathrm{dc} /} / \mathrm{I}_{\mathrm{av}}=\mathrm{Im} / \pi \\
& \mathrm{I}_{\mathrm{rms}}=\mathrm{I}_{\mathrm{m}} / 2 \\
& \mathrm{P}_{\mathrm{dc}}=\mathrm{I}_{\mathrm{dc}}^{2} \cdot \mathrm{R}_{\mathrm{L}}=\left(\mathrm{I}_{\mathrm{m}} / \mathrm{pi}\right)^{2} \mathrm{R}_{\mathrm{L}} \\
& \mathrm{P}_{\mathrm{ac}}=\mathrm{I}_{\mathrm{r} \mathrm{~ms}}{ }^{2}\left(\mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right)=\left(\mathrm{I}_{\mathrm{m}} / 2\right)^{2}\left(\mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right)
\end{aligned}
$$

Hence Efficiency $\eta=\mathrm{P}_{\mathrm{dc}} / \mathrm{P}_{\mathrm{ac}}=\left(\mathrm{I}_{\mathrm{m}} / \mathrm{pi}\right)^{2} \mathrm{R}_{\mathrm{L}} /\left(\mathrm{I}_{\mathrm{m}} / 2\right)^{2}\left(\mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right)=\left(4 / \mathrm{pi}^{2}\right)\left(\mathrm{R}_{\mathrm{L}} / \mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right)=\left(4 / \mathrm{pi}^{2}\right)\left(1 / 1+\mathrm{r}_{\mathrm{f}} / \mathrm{RL}\right)$

$$
=0.405 x\left(1 / 1+\mathrm{r}_{f} / \mathrm{RL}\right)
$$

Since $\mathrm{rf} / \mathrm{RL} \ll 1, \mathrm{f} /$ /RL can be neglected.
Finally, $\eta=0.405=40.5 \%$

## RFECTELER EFFICIENCY OF FULL WAVE RECTIFIER:

## Forfull wave rectifier, $\quad \mathrm{I}_{\mathrm{dc}} / \mathrm{I}_{\mathrm{av}}=2 \mathrm{Im} / \pi$

$$
\begin{aligned}
& \mathrm{I}_{\mathrm{rms}}=\mathrm{Im} / \sqrt{2} \\
& \mathrm{P}_{\mathrm{dc}}=\mathrm{I}_{\mathrm{dc}}{ }^{2} \cdot \mathrm{R}_{\mathrm{L}}=\left(2 \mathrm{I}_{\mathrm{m}} / \mathrm{pi}\right)^{2} \mathrm{R}_{\mathrm{L}}
\end{aligned}
$$

$$
\begin{aligned}
& \mathrm{P}_{\mathrm{ac}}=\mathrm{Irms}^{2}\left(\mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right)=\left(\mathrm{I}_{\mathrm{m}} / \sqrt{2}\right)^{2}\left(\mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right) \\
& \text { Hence Efficiency, } \quad \begin{aligned}
\eta=\mathrm{P}_{\mathrm{dc}} / \mathrm{P}_{\mathrm{ac}} & =\left(2 \mathrm{I}_{\mathrm{m}} / \mathrm{pi}\right)^{2} \mathrm{R}_{\mathrm{L}} /\left(\mathrm{I}_{\mathrm{m}} / \sqrt{2}\right)^{2}\left(\mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right)=\left(8 / \mathrm{pi}^{2}\right)\left(\mathrm{R}_{\mathrm{L}} / \mathrm{R}_{\mathrm{L}}+\mathrm{r}_{\mathrm{f}}\right)=\left(8 / \mathrm{pi}^{2}\right)\left(1 / 1+\mathrm{r}_{\mathrm{f}} / \mathrm{RL}\right) \\
& =0.810\left(1 / 1+\mathrm{r}_{\mathrm{f}} / \mathrm{RL}\right)
\end{aligned}
\end{aligned}
$$

Since $\mathrm{rf} / \mathrm{RL} \ll 1, \mathrm{rf} / \mathrm{RL}$ can be neglected.
Finally, $\quad \eta=0.810=81 \%$

## RIPPLE:

The amount of ac component present in rectifier output signal is called ripple.

## RIPPLE FACTOR:

The ratio of r.m.s. value of ac component to dc component of rectifier output is called rectifier efficiency.
i.e. ripple factor, $\gamma=\mathrm{Iac} / \mathrm{I}_{\mathrm{dc}}$

Basically the total current is given by: $\mathrm{I}_{\mathrm{ac}}{ }^{2}=\mathrm{I}_{\mathrm{rms}}{ }^{2}+\mathrm{I}_{\mathrm{dc}}{ }^{2}$

$$
\begin{aligned}
& \mathrm{I}_{\mathrm{rms}}=\mathrm{I}_{\mathrm{ac}}{ }^{2}-\mathrm{I}_{\mathrm{dc}}{ }^{2} \\
& \mathrm{I}_{\mathrm{rms}}^{2} / \mathrm{Idc}_{\mathrm{dc}}=\left(\mathrm{I}_{\mathrm{ac}}{ }^{2}-\mathrm{I}_{\mathrm{dc}}{ }^{2}\right) / \mathrm{I}_{\mathrm{dc}}{ }^{2} \\
& \gamma^{2}=\left(\mathrm{I}_{\mathrm{ca}} / \mathrm{I}_{\mathrm{dc}}\right)^{2}-1 \\
& \gamma=\sqrt{\left(\frac{\mathrm{Iac}}{I d c}\right) 2-1}
\end{aligned}
$$

## IMPORTANT TERMS IN DIODE:

## *BREAK DOWN VOLTAGE:

$>$ The voltage under reverse bias condition at which current suddenly rises to high value is called break down voltage.
$>$ At breakdown voltage the diode is not behaving as a diode
$>$ The region over which this occurs is called breakdown tégion.
>There are two types of breakdown voltage
(a) Avalanche Breakdown Voltage
(b)Zener Breakdown Voltage

## *PIV/PRV (Peak Inverse Voltage/Peak Reverse voltage) :

>It is the maximum reverse voltage that gan be given to a diode just before entering to the breakdown region.
>It is the maximum safe operating yoltage of diode.
*KNEE VOLTAGE:
$>$ It is the minimum forward yoltage after which current rises rapidly with voltage.
$>$ Its value is 0.7 v for $\mathrm{S}_{1} \& 0.3 \mathrm{v}$ for Ge .

## COMPARISION BETWEEN AVALANCHE BREAKDOWN \& ZENER BREAKDOWN

## AVALANCHE BREAKDOWN

1-This breakdown occurs due to higher across
velocity of minority carriers.
2-This occurs in a diode with lower doping level.
3-It occurs at higher reverse voltage.
4-This breakdown is not sharp.
5-It occurs in general diode.

1-This occurs due to stronger electric field the diode.
2-It occurs in a heavily doped diode.
3-It occurs at lower reverse voltage.
4-This breakdown is sharp.
5-It occurs in zener diode.

## CHAPTER-3 <br> FILTER CIRCUITS

## FILTER:

$>$ The device which converts pulsating dc to pure dc is called filter.
$>$ Figure:



Basically consists of capacitors \& inductors.

## TYPES OF FILTER:

There are three types of filters:
(a)capacitor filter
(b) choke input filter
(c)Pi-filter

## CAPACITOR FILTER:



## Circuit Detail:

It consists of capacitor $C$ \& load resistor $R_{L}$. Capacitor $C$ used for filtering purpose. The pure dc output develops acros load resistor $\mathrm{R}_{\mathrm{L}}$.

## Operation

$>$ When the pulsating dc is applied input is applied across the input terminal, it produces a pulsating dq eurrent $\mathrm{I}=\mathrm{I}_{\mathrm{ac}}+\mathrm{I}_{\mathrm{dc}}$.
Where $\mathrm{I}_{\mathrm{ac}}=\mathrm{ac}$ component current
$\mathrm{I}_{\mathrm{dc}}=\mathrm{dc}$ component current
$>$ When this current I face capacitor C, capacitor C opposes the dc component \& bypass the ac component through it. As a result the dc component current flows towards load resistor RL. In this way pulsatig dc is converted to pure dc.
> Input \& output wave form:

(b) Full-wave

## CHOKE INPUT FILTER:

## Circuit Diagram:



## Circuit Detail:

It consists of choke L \& capacitor c \& load resistor $R_{L}$. Choke L \& capacitor C used for filtering purpose. The pure do outpat develops across load resistor $\mathrm{R}_{\mathrm{L}}$.

## Operation:

$>$ When the pulsating dc input is applied across the input, it produces pulsating current $\mathrm{I}=\mathrm{I}_{\mathrm{ac}}+\mathrm{I}_{\mathrm{dc}}$. This mixing signal when flows through choke L , it opposes blocks ac components \& allows through it the dc component.But the choke L can not able to block all the ac components. As a result at the output of the choke we get again dc component with some ac component.The output current of choke when face the capacitor C , the remaining ac component bypasses through it.But the dc component blocked by C. As a result the dc component flows towards load resistor RL.In this way pulsating dc is converted to pure dc.
It is clear from the output signal that the variation is less than the capacitor input filter in the output. Hence this filter provides better dc as compared to capacitor input filter.

Input output wave form :




RECTIFIER OUTPUT

PI-FILTER/CAPACITOR INPUT FILTER:

## Circuit Diagram:

L

$>$ The choke L offers high reactance to the ac component \& almost zero reactance to the dc component. Hence it allows the dc component to flow through it \& blocks the ac component not able to bypassed by $\mathrm{C}_{1}$.

## CHAPTER-4 Bipolar Junction Transistor

## TRANSISTOR:

The electronic device in which a dissimilar type of semiconductor material is sandwiched between two similar type of semiconductor is called transistor.
In this either a p-type is sandwiched between two n-type or an n-type is sandwiched between two p-type material.
Transistor consists of two words: transistor. Trans means the signal transfer propertyof the device \& istor means resistor property of the device.
A transistor transfers a signal from a low resistance to high resistance.

## TYPES OF TRANSISTOR:

There are two types of transistors:
a) n-p-n transistor
b) $p-n-p$ transistor
> Structure \& Symbol:



(b)
$>$ It has three terminals, one taken from each type of semiconductor. The terminals are named as base(B), emitter(E), collector(C).
It has two pn-junction \& three semiconductor layers.
TERMINALS OF TRANSISTOR:
It has three terminals, named as base, emitter \& collector. The two end terminals are known as emitter(E) \& collector(C), middle is called as base.

## Emitter:

a) This layer provides charge carriers.
b) It is always forward biased w.r.t. base.
c) It is wider than base.
d) It is heavily doped. Hence it provides large numbers of charge carriers into base.

## Base:

a) This layer controls the amount of charge carrier flow from emitter to collector.
b) It is forward connected w.r.t. emitter \& reverse biased w.r.t. collector.
c) It is much thinner than emitter.
d) It is lightly dopped. Hence it passes most of the charge carriers coming from emitter to collector.

Collector:
a) This layer removes charges from its junction with the base.
b) It is reverse biased w.r.t. base.
c) It is wider than emitter $\&$ base.
d) It is moderately doped.

## WORKING PRINCIPLE OF NPN TRANSISTOR:

*Figure shows the circuit for showing the working principle.


## Basic connection of npn transistor

*For proper operation of transistor, base emitter junction is forward biased by $\mathrm{V}_{\mathrm{EE}} \&$ base-collector is reverse biased by $\mathrm{V}_{\mathrm{Cc}}$.
*The n-type emitter has majority free electrons. The forward bias on emitter, causes the free electrons in the n-type emitter toflow towards the base. This constitutes the emitter current $\mathrm{I}_{\mathrm{E}}$.
*When the free electrons flows through p-type base, they try to combine with majority holes in base resion. Since the base is lightly doped \& very thin, only a few electrons combine with holes \& constitute base current $\mathrm{I}_{\mathrm{B}}$.
*The remining free electrons flows towards the collector attracted by strong positive terminal of the biasing supply $+\mathrm{V}_{\mathrm{cc}}$. This constitute the collector current $\mathrm{I}_{\mathrm{C}}$.
*Itis glear that almost the entire emitter current flows in the collector circuit. Hence emitter current is the sum of collector \& base current i.e.

$$
\mathrm{I}_{\mathrm{E}}=\mathrm{I}_{\mathrm{B}}+\mathrm{I}_{\mathrm{C}}
$$

*The current conduction within the transistor is due to free electrons \& also through the external circuit is due to free electrons.
*For proper operation of transistor, base emitter junction is forward biased by $\mathrm{V}_{\mathrm{EE}} \&$ base-collector is reverse biased by $\mathrm{V}_{\mathrm{Cc}}$.
*The p-type emitter has majority holes. The forward bias on emitter, causes the holes in the p-type emitter to flow towards the base.This constitutes the emitter current $\mathrm{I}_{\mathrm{E}}$.
*When the holes flows through n-type base, they try to combine with majority free electrons in base resion. Since the base is lightly doped \& very thin, only a few holes combine with free electrons \& constitute base current $\mathrm{I}_{\mathrm{B}}$.
*The remaining holes flows towards the collector attracted by strong negative terminal of the biasing supply $-\mathrm{V}_{\mathrm{cc}}$. This constitute the collector current $\mathrm{I}_{\mathrm{C}}$.
*It is clear that almost the entire emitter current flows in the collector circuit. Hence emitter current is, the sum of collector \& base current i.e.

$$
\mathrm{I}_{\mathrm{E}}=\mathrm{I}_{\mathrm{B}}+\mathrm{I}_{\mathrm{C}}
$$

*The current conduction within the transistor is due to holes \& through the external circuit is due to free electrons.

## TRANSISTOR CONNECTION:

There are three types of connections:
a) Common- Base Connection(CB)
b) Common-Emitter Connection(CE)
c) Common-Collector Connection(CC)

## COMMON-BASE CONNECTION:

* The transistor connection in which base is common for both input \& output circuit is called commonbase connection.
*In this input is applied between emitter \& base \& outpet is taken from collector \& base.
*Circuit Diagram:




## Common base configuration

*D.C. supply $\mathrm{V}_{\mathrm{EE}}$ provides forward biasing \& $\mathrm{V}_{\mathrm{cc}}$ providés reyerse biasing.

## COMMON-EMITTER CONNECTION

* The transistor connection in which emitter is common for both input \& output circuit is called common-emitter connection.
*In this input is applied between emitter \& base \& output is taken from collector \& emitter.
*Circuit Diagram:



*D.C. supply $\mathrm{V}_{\text {вв }}$ provides forward biasing \& $\mathrm{V}_{\mathrm{cc}}$ provides reverse biasing.


## COMMON-COLLECTOR CONNECTION:

* The transistor connection in which collector is common for both input \& output circuit is called common-collector connection.
*In this input is applied between base \& collector \& output is taken from collector \& emitter.
*Circuit Diagram:

*D.C. supply $\mathrm{V}_{\text {вв }}$ provides forward biasing across base to collector \& $\mathrm{V}_{\mathrm{cc}}$ provides reverse biasing across emitter to collector.


## CURRENT AMPLIFICATIONTACTOR IN COMMON BASE CONNECTION( $\alpha$ ):

*The ratio between change in collector current to change in emitter current at constant collector to base voltage $\mathrm{V}_{\mathrm{CB}}$ is called current amplification factor $\alpha$.
*Mathematically, $\alpha=\Delta \mathrm{IC} \Delta \mathrm{IE}_{\mathrm{E}}$ at constant $\mathrm{V}_{\mathrm{CB}}$
*Its value is less than unity. Practical values of $\alpha$ ranges from 0.9 to 0.99 .

## CURRENT AMPLIFICATION FACTOR IN COMMON EMITTER ( $\beta$ ):

*The ratio betweenthange in collector current to change in base current at constant collector to emitter voltage $V_{Q}$ is called current amplification factor $\beta$.
*Mathenatically, $\beta=\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{B}}$ at constant $\mathrm{V}_{\mathrm{CE}}$
*Its value is greater than 20. Practical values of $\beta$ ranges from 20 to 500 .

## CURRENT AMPLIFICATION FACTOR IN COMMON COLLECTOR(Y)

*The ratio between change in emitter current to change in base current at constant collector to emitter voltage $\mathrm{V}_{\mathrm{CE}}$ is called current amplification factor $\beta$.
*Mathematically, $\mathrm{Y}=\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{B}}$ at constant $\mathrm{V}_{\mathrm{CE}}$
*Its value is greater than 20. Practical values of $\beta$ ranges from 20 to 500 i.e. same as common emitter value.
RELATION BETWEEN $\alpha \& \beta$ :
We know $\beta=\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{B}}$
$\alpha=\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{E}}$
$\mathrm{I}_{\mathrm{E}}=\mathrm{I}_{\mathrm{B}}+\mathrm{I}_{\mathrm{C}}$
$\Delta \mathrm{I}_{\mathrm{E}}=\Delta \mathrm{I}_{\mathrm{B}}+\Delta \mathrm{I}_{\mathrm{C}}$
Hence $\Delta \mathrm{I}_{\mathrm{B}}=\Delta \mathrm{I}_{\mathrm{E}}-\Delta \mathrm{I}_{\mathrm{C}}$
Substituting the values of $\Delta \mathrm{I}_{\mathrm{B}}$ in equation (1), we get, $\beta=\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{E}}-\Delta \mathrm{I}_{\mathrm{C}}$
Dividing both numerator \& denominator by $\Delta \mathrm{I}_{\mathrm{E}}$ of R.H.S. in eqn.(3),

$$
\beta=\left(\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{E}}\right) /\left(\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{E}}\right)-\left(\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{E}}\right)=\alpha /(1-\alpha)
$$

$\beta=\alpha / 1-\alpha$

## RELATION BETWEEN Y \& $\alpha$ :

We know
$\mathrm{Y}=\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{B}}$
$\alpha=\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{E}} \ldots$
$\Delta \mathrm{I}_{\mathrm{E}}=\Delta \mathrm{I}_{\mathrm{B}}+\Delta \mathrm{I}_{\mathrm{C}}$
Hence $\quad \Delta \mathrm{I}_{\mathrm{B}}=\Delta \mathrm{I}_{\mathrm{E}}-\Delta \mathrm{I}_{\mathrm{C}}$
Substituting the value of $\Delta \mathrm{I}_{\mathrm{B}}$ in eqn. (4),

$$
\begin{equation*}
\mathrm{Y}=\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{B}}=\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{E}}-\Delta \mathrm{I}_{\mathrm{C}} . \tag{6}
\end{equation*}
$$

Dividing both numerator $\&$ denominator by $\Delta \mathrm{I}_{\mathrm{E}}$ of eqn.
$\mathrm{Y}=\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{B}}=\left(\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{E}}\right) /\left(\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{E}}\right)-\left(\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{E}}\right)=1 / 1-\alpha$
$\mathrm{Y}=1 / 1-\alpha$

## RELATION BETWEEN $\boldsymbol{\alpha}, \boldsymbol{\beta}$ \& Y:

We know

$$
\begin{equation*}
\alpha=\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{E}} . \tag{7}
\end{equation*}
$$

$\beta=\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{B}}$
$\mathrm{Y}=\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{B}}$
Multiplying $\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{E}}$ in R.H.S. of eqn. (8),
$\beta=\left(\Delta \mathrm{I}_{\mathrm{C}} / \Delta \mathrm{I}_{\mathrm{B}}\right) \mathrm{x}\left(\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{E}}\right)=\left(\Delta \mathrm{I} / \Delta \mathrm{I}_{\mathrm{F}}\right) \mathrm{x}\left(\Delta \mathrm{I}_{\mathrm{E}} / \Delta \mathrm{I}_{\mathrm{B}}\right)=\alpha . \mathrm{Y}$
$\beta=\alpha . Y$

## COMMON BASE TRANSISTOR AMPLIFIER:

*Circuit diagram

*Circuit Details:
It consists of transistor Q , load resistor $\mathrm{R}_{1}$, biasing supply $\mathrm{V}_{\mathrm{EE}} \& \mathrm{~V}_{\mathrm{CC}}$.
Transistor Q used for amplification. Amplified output develops across load resistor Rk
$\mathrm{V}_{\mathrm{EE}}$ provides proper forward biasing across emitter to base.
$\mathrm{V}_{\mathrm{CC}}$ provides proper reverse biasing across collector to base.
Vi is the input supply to be amplified.
Vo is the amplified output.
*Circuit operation:
When the input signal to be amplified is applied across the emitter to base, for a small change in input we get a large change in output current. This large change in current when flows through a high load resistance Rl, produces a large voltage drop across Rl. Now if we compare the input voltage \& output voltage, output is more than the input. In this way we get amprified output.

## COMMON EMITTER AMPLIFIER:

*Circuit diagram:

*Circuit details:
It consists of transistor Q , load resistor $\mathrm{R}_{1}$, biasing supply $\mathrm{V}_{\mathrm{BB}} \& \mathrm{~V}_{\mathrm{CC}}$.

Transistor Q used for amplification. Amplified output develops across load resistor R1.
$V_{\text {bв }}$ provides proper forward biasing across emitter to base.
$\mathrm{V}_{\mathrm{CC}}$ provides proper reverse biasing across collector toemitter.
$\mathrm{V}_{\mathrm{i}}$ is the input supply to be amplified.
$\mathrm{V}_{\mathrm{o}}$ is the amplified output.
*Operation:

1) During the positive half cycle of the input signal, forward bias across the emitter-base junction is increased. Hence more electrons flow from the emitter to the collector through the base. This causes an increase in collector current. The increased collector current when flows through a high load resistance $\mathrm{R}_{\mathrm{l}}$, produces high voltage drop.
2) During the negative half cycle of the input signal, the forward bias across emitter-base junction is decreased. Hence collector current decreases. This decreased collector current when flows through load resistance, produces decreased output voltage in opposite direction. Hence an amplified outpat is obtained across the load.

## V-I CHARACTERISTIC OF COMMON BASE TRANSISTOR CONNECTION:

Two types of V-I characteristic,
a) Input V-I characteristic
b) Output V-I characteristic

## INPUT V-I CHARACTERISTIC OF CB:

*The graph which shows the relation between emitter current $\mathrm{I}_{\mathrm{E}}$ \& emitter-base voltage $\mathrm{V}_{\mathrm{EB}}$ at constant collector-base voltage $\mathrm{V}_{\mathrm{CB}}$ is called input characteristic.
$* \mathrm{~V}_{\mathrm{EB}}$ is taken along x -axis \& $\mathrm{I}_{\mathrm{E}}$ is taken along y-axis.
*Graph:

*It is clear from the graph that, emitter current $\mathrm{I}_{\mathrm{E}}$ increases rapidly with small increase in emitter-base voltage $\mathrm{V}_{\mathrm{Eb}}$.
*The emitter current is almost independent of collector-base voltage $\mathrm{V}_{\mathrm{CB}}$.

## OUTPUT V-I CHARACTERISTIC OF CB:

*The graph which shows the relation between collector current $\mathrm{I}_{\mathrm{c}}$ \& collector-base voltage VCBaty constant emitter current $\mathrm{I}_{\mathrm{E}}$ is called output characteristic.

* $V_{\mathrm{CB}}$ is taken along x -axis \& $\mathrm{I}_{\mathrm{c}}$ is taken along y -axis.
*Graph:


O/P characteristics CB configuration
*It is clear from the graph that,
a) Collector current cvaries with $\mathrm{V}_{\mathrm{CB}}$ only at very low voltage (<1V).
b) For $\mathrm{V}_{\mathrm{CB}}$ greater than 1 V , collector current remains constant.
c) A verydarge change in collector-base voltage produces only a small change in collector current.

## V-ICHARACTERISTIC OF COMMON-EMITTER CONNECTION:

There are two types of V-I characteristic:

1) Input V-I Characteristic
2) Output V-I characteristic

## INPUT V-I CHARACTERISTIC OF CE:

*The graph which shows the relation between base current $\mathrm{I}_{\mathrm{B}}$ \& base-emitter voltage $\mathrm{V}_{\mathrm{BE}}$ at constant collector emitter voltage $\mathrm{V}_{\mathrm{CE}}$ is called input characteristic.
$* V_{B E}$ is taken along $x$-axis \& $I_{B}$ is taken along $y$-axis.
*Graph:


I/P characteristics CE configuration
*It is clear from the graph that,
a) The characteristic is smilar to characteristic of forward biased pn-junction.
b) At first current IB increases very slowly. After certain voltage known as knee voltage, the current increases rapidly.

## OUTPUT $\begin{gathered}\text { I } \\ \text { I CHARACTERISTIC OF CE: }\end{gathered}$

*The graph which shows the relation between collector current $I_{c}$ \& collector-emitter voltage $V_{C E}$ at constant base current $\mathrm{I}_{\mathrm{B}}$ is called output characteristic.

* $\mathrm{V}_{\text {CE }}$ is taken along x-axis \& $\mathrm{I}_{\mathrm{c}}$ is taken along y -axis.
*Graph:


It is clear from the graph that,
a) Collector current $I_{C}$ varies with $V_{C E}$ only at very low voltage $(\mathbb{V})$.
b) For $\mathrm{V}_{\mathrm{CE}}$ greater than 1 V , collector current remains constânt.
c) A very large change in collector-emitter voltage produces only a small change in collector current.

## TRANSISTOR DC LOAD LINE:

$>$ It is a method of measuring collector current $\mathrm{I}_{\mathrm{C}}$ for different values of collector-emitter voltage accurately.
$>$ Circuit for getting dc load line.


> Appling output KVL:
$\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CE}}+\mathrm{I}_{\mathrm{C}} \mathrm{R}_{\mathrm{C}}$
$\mathrm{V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{CC}}-\mathrm{I}_{\mathrm{C}} \mathrm{R}_{\mathrm{C}}$
This equation is in the form of a straight line. Hence its graph is a straight line $\&$ can be drawn on output characteristics. The graph can be drawn as follows:
a) If $\mathrm{I}_{\mathrm{C}}=0$, then equation (10) is: $\mathrm{V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{CC}}$

This forms the coordinate $\left(\mathrm{V}_{\mathrm{CE}}, \mathrm{I}_{\mathrm{C}}\right)=\left(\mathrm{V}_{\mathrm{CC}}, 0\right)$. This point is indicated by the point A on $\mathrm{V}_{\mathrm{CE}}$ axis.
b) Putting $\mathrm{V}_{\mathrm{CE}}=0$ in eqn. (10):

$$
0=\mathrm{V}_{\mathrm{CC}}-\mathrm{I}_{\mathrm{C}} \mathrm{R}_{\mathrm{C}}
$$

i.e. $\mathrm{I}_{\mathrm{C}}=\mathrm{V}_{\mathrm{C}} / \mathrm{R}_{\mathrm{C}}$

This forms the coordinate $\left(V_{C E}, I_{C}\right)=\left(\theta, V_{C C} / R_{C}\right)$. This point is indicated by the point $B$ on $I_{C}$ axis.
By joining the points A \& B , the straight line AB is called dc load line.

## OPERATING POINT:

$>$ The zero signal values of collector current $\mathrm{I}_{\mathrm{C}} \&$ collector -emitter voltage $\mathrm{V}_{\mathrm{CE}}$ is called operating point.
$>$ The intersection of output V-I characteristic \& dc load line is also called operating point.
$>$ Also named as Q-point or quiescent point.


## IMPORTANT SITUATIONS OF TRANSISTOR:

a) CUT OFF:

The point where the load line intersects the $\mathrm{I}_{\mathrm{B}}=0$ curve is known as cut off. The region below this point is called cut off region.
At cut off both input \& output side is reverse biased \& transistor action is lost.
b) Saturation :The point where the load line intersects the $\mathrm{I}_{\mathrm{B}}=\mathrm{I}_{\mathrm{B}}($ sat $)$ curve is called saturation . The region above this is called saturation region.
At saturation both input \& output side is forward biased \& normal transistor action is lost.
c) ACTIVE REGION: The region between cut off \& saturation is cated active region. In this region input is forward biased \& output is reverse biased. The transistoraction is normal.


| S. No. | Characteristic | Common base | Common emitter | Common collector |
| :---: | :---: | :---: | :---: | :---: |
| 1. | Input resistance | Low (about $100 \Omega$ ) | Low (about $750 \Omega$ ) | Very high (about $750 \mathrm{k} \Omega$ ) |
| 2. | Output resistance | Very high (about $450 \mathrm{k} \Omega$ ) | High (about $45 \mathrm{k} \Omega$ ) | Low (about $50 \Omega$ ) |
| 3. | Voltage gain | about 150 | about 500 | less than 1 |
| 4. | Applications | For high frequency applications | For audio frequency applications | For impedance matching |
| 5. | Current gain | No (less than 1) | High ( $\beta$ ) | Appreciable |

## CHAPTER-5

‘

## TRANSISTOR BIASING

## Transistor biasing:

$>$ The proper flow of zero signal collector current \& the maintenance of proper collector-emitter voltage during the passage of signal is called as transistor biasing.
$>$ The purpose of biasing is to make base-emitter junction properly forward biased \& collector-base junction reverse biased during the application of signal.

## STABILISATION:

$>$ The process of making operating point independent of temperature changes or variation in transistor parameters is known as stabilisation.

## NEED OF STABILISATION:

Stabilisation of the operating point is necessary due to the following reasons:
a)Temperature dependence of IC.
b) Individual variations.
c) Thermal runaway.

METHODS OF TRANSISTOR BIASING:
a) Base resistor method
b) Emitter bias method
c) Feedback resistor method
d) Voltage divider bias method

BASE RESISTOR METHOD:
$>$ Circuit diagram:


In this method a high resistance $\mathrm{R}_{\mathrm{B}}$ is connected between the base \& +ve end of supply for npn transistor \& between base \& negative end of supply for pnp transistor. This provides the input biasing.
$+V_{\text {CC }}$ is the biasing supply. $\mathrm{R}_{\mathrm{C}}$ is the collector load.
Circuit Analysis:
The required zero signal base current is provided by $+V_{C C} \&$ it flows through $R_{B}$. This makes base terminal positive \& produces proper forward biasing across base -emitter junction. The proper zero signal base current $\mathrm{I}_{\mathrm{B}} \&$ also collector current $\mathrm{I}_{\mathrm{C}}$ depends on proper value of base

> resistor $\mathrm{R}_{\mathrm{B}}$.
> $\mathrm{I}_{\mathrm{C}}=\beta . \mathrm{I}_{\mathrm{B}}$
> Applying input KVL,
> $\mathrm{V}_{\mathrm{CC}}=\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{B}}+\mathrm{V}_{\mathrm{BE}}$
> $\mathrm{R}_{\mathrm{B}}=\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{BE}}\right) / \mathrm{I}_{\mathrm{B}}$

## Advantages:

1-The circuit is very simple.
2-Requirs simple calculations.
3-There is no loading of the source, because no resistor is employed across base-emitter junction.

## Disadvantages:

1-This method provides poor stabilization.
2-This method isles stable.
3-There is a chance of thermal runway.

## Emitte-Biasing

Circuit diagram:

> Circuit detail:
In this method a high resistance $R_{B}$ is connected between the base \& +ve end of supply for npn transistor \& between-base \& negative end of supply for pnp transistor. This provides the input biasing.
$+\mathrm{V}_{\mathrm{CC}}$ is the biasing supply. $\mathrm{R}_{\mathrm{C}}$ is the collector load. $\mathrm{R}_{\mathrm{E}}$ is the emitter resistor \& it provides
stabilization
$>$ Circuit analysis.
The required zero signal base current is provided by $+\mathrm{V}_{\mathrm{CC}} \&$ it flows through $\mathrm{R}_{\mathrm{B}}$. This makes base terminal positive \& produces proper forward biasing across base -emitter junction. The propey zero signal base current $I_{B} \&$ also collector current $I_{C}$ depends on proper value of base resistor $R_{B}$.
${ }_{\mathrm{I}}=-\beta . \mathrm{I}_{\mathrm{B}}$
Applying input KVL,
$\mathrm{V}_{\mathrm{CC}}=\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{B}}+\mathrm{V}_{\mathrm{BE}}+\mathrm{I}_{\mathrm{E}} \mathrm{R}_{\mathrm{E}}=\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{B}}+\mathrm{V}_{\mathrm{BE}}+(\beta+1) \mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{E}}=\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{B}}+\mathrm{V}_{\mathrm{BE}}+\beta \mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{E}}$
$\mathrm{I}_{\mathrm{B}}=\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{BE}}\right) / \mathrm{R}_{\mathrm{B}}+\mathrm{R}_{\mathrm{E}}$

## FEEDBACK RESISTOR METHOD:

## Circuit diagram:



Circuit Details:
In this method a high resistance $R_{B}$ is connected between the base \& collector of transistor. This provides the input biasing.
$+\mathrm{V}_{\mathrm{CC}}$ is the biasing supply. $\mathrm{R}_{\mathrm{C}}$ is the collector load.
$>$ Circuit analysis:
The required zero signal base current is provided by cotlector-base voltage $\mathrm{V}_{\mathrm{CB}}$ but not by $+\mathrm{V}_{\mathrm{CC}} \&$ it flows through $R_{B}$. This makes base terminal positive \& produces proper forward biasing across base emitter junction. The proper zero signal base current $\mathrm{I}_{\mathrm{B}} \&$ also collector current $\mathrm{I}_{C}$ depends on proper value of base resistor $\mathrm{R}_{\mathrm{B}}$.
$\mathrm{I}_{\mathrm{C}}=\beta . \mathrm{I}_{\mathrm{B}}$
Applying input KVL,
$\mathrm{V}_{\mathrm{CC}}=\left(\mathrm{I}_{\mathrm{C}}+\mathrm{I}_{\mathrm{B}}\right) \mathrm{R}_{\mathrm{C}}+\mathrm{I}_{\mathrm{B}} \mathrm{R}_{\mathrm{B}}+\mathrm{V}_{\mathrm{BE}}$
$\mathrm{R}_{\mathrm{B}}=\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{BE}-\mathrm{I}} \mathrm{I}_{\mathrm{C}} \mathrm{R}_{\mathrm{C}}\right) / \mathrm{I}_{\mathrm{B}}$
ADVANTAGES:
1 -It is a simple method.
2-It provides better stabilization than fixed bias method.

## DISADVANTAGES:

1-This circuit does not provide good stabilization.
2-It provides negative feedback which reduces the gain of amplifier.

## VOLTAGE DHIDER METHOD OF BIASING:

[^1]
> Circuit details:
In this a single battery supply $\mathrm{V}_{\mathrm{CC}}$ is used to provide biasing to both input \& output side Resistor $\mathrm{R}_{1}-\mathrm{R}_{2}$ provides proper forward biasing to base. Biasing supply $\mathrm{V}_{\mathrm{CC}}$ provides directly biasing to collector. Emitter resistance $R_{E}$ used for biasing \& stabilization. Emitter bypass capacitor CE bypasses the a.c. component of emitter current.
$>$ Circuit analysis:
In this $\quad V_{2}=\left(V_{C C} / R_{1}+R_{2}\right) \times R_{2}$
$$
\mathrm{V}_{\mathrm{BE}}=\mathrm{V}_{2}-\mathrm{I}_{\mathrm{E}} \mathrm{R}_{\mathrm{E}}
$$
$\mathrm{I}_{\mathrm{E}}=\mathrm{V}_{2}-\mathrm{V}_{\mathrm{BE}} / \mathrm{R}_{\mathrm{E}}$
$\mathrm{V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{CC}}-\mathrm{I}_{\mathrm{C}}\left(\mathrm{R}_{\mathrm{C}}+\mathrm{R}_{\mathrm{E}}\right)$

## CHAPTER-6

## FEEDBACK AMPLIFIER

## FEED BACK:

The process of applying a fraction of output energy of some device back to the input is known as feedback.

## FEEDBACK AMPLIFIER:

The amplifier using feed back process is called feedback amplifier.


## TYPES OF FEEDBACK AMPLIFIER:

There are two types of feedback amplifier:
a) Positive feedback amplifier
b) Negative feedback amplifier

## POSITIVE FEEDBACK AMPLIFIER:

$>$ The amplifier in which feedback energy is applied in the same polarity or in same phase is called as positive feedback amplifier.
$>$ It increases the voltage gain of amplifier.
$>$ In this distortion is more.
$>$ It has increased instability.
> It seldom used as an aphnlifier. Mostly used in oscillator.

## NEGATIVE FEEDBACK AMPLIFIER:

$>$ The amplifier in which feedback energy is applied in the opposite polarity or out of phase with input is called regative feedback amplifier.
$>$ It decreases the voltage gain.
$>$ In thisis distortion is less.
$>$ Iris more stable.
$>$ It is mostly used as an amplifier.

## PRINCIPLE OF NEGATIVE FEEDBACK AMPLIFIER:

> Block diagram of negative feedback amplifier:

$>\mathrm{A}=$ Voltage gain without feedback.
$\mathrm{A}_{\mathrm{f}}=$ voltage gain with feedback.
Vs=Input signal to be amplified.
$\mathrm{V}_{\mathrm{o}}=$ Output signal of amplifier
$\mathrm{Vi}=$ Actual input signal to the amplifier.
$\mathrm{V}_{\mathrm{f}}=$ Feedback signal applied to input side.
$\beta=$ feedback fraction
$>$ From block diagram it is clear that,
$\beta=\mathrm{V}_{\mathrm{f}} / \mathrm{V}_{\text {o }}$ i.e. $\mathrm{V}_{\mathrm{f}}=\beta \mathrm{V}_{\text {o }}$
$\mathrm{Vi}=\mathrm{Vs}_{\mathrm{s}}-\mathrm{V}_{\mathrm{f}}=\mathrm{Vss}_{\mathrm{s}}-\beta \mathrm{V}_{\mathrm{o}}$
Again $\mathrm{A}=\mathrm{V}_{\mathrm{o}} / \mathrm{Vi}$ i.e. $\mathrm{V}_{\mathrm{o}}=\mathrm{AVi}=\mathrm{A}\left(\mathrm{Vs}-\beta \mathrm{V}_{\mathrm{o}}\right)$ i.e. $V_{o}=A V s-A \beta V_{o}$
i.e. $V_{0}+A \beta V_{o}=A V s$
i.e. $V_{0}(1+\beta A)=A V s$
$\mathrm{V}_{\mathrm{o}} / \mathrm{Vs}=\mathrm{A} /(1+\beta \mathrm{A})$
$\mathrm{A}_{\mathrm{f}}=\mathrm{A} /(1+\beta \mathrm{A})$
It is clear that voltage gain with feedback decreases by a factor $(1+\beta A)$.
ADVANTAGES OF NEGATIVE FEEDBACK, AMPLIFIER:
> Resultant gain is independent of transistor parameters or supply voltage fluctuation. Hence gain is stable.
$>$ It reduces non-linear distortion bra factor $(1+\mathrm{mA})$.
$>$ It improves frequency response.
$>$ It increases circuit stability
$>$ It increases input impedance \& decreases output impedance.

## INPUT IMPEDANCE \& OUTPUT IMPEDANCE WITH FEEDBACK:

> Figure shows the block diagram:


## $>$ Given that:

$\mathrm{A}=$ Voltage gain without feedback.
$\mathrm{A}_{\mathrm{f}}=$ voltage gain with feedback.
Vs=Input signal to be amplified.
$\mathrm{V}_{\mathrm{o}}=$ Output signal of amplifier
$\mathrm{Vi}=$ Actual input signal to the amplifier.
$\mathrm{V}_{\mathrm{f}}=$ Feedback signal applied to input side.
$\beta=$ feedback fraction
$\mathrm{Z}_{\mathrm{i}}=$ input impedance without feedback= $\mathrm{Vi} / \mathrm{i}_{\mathrm{i}}$
$\mathrm{Z}_{\mathrm{if}}=$ Input impedance with feedback= $\mathrm{Vs} / \mathrm{i}_{\mathrm{i}}$
$\mathrm{Z}_{\mathrm{o}}=$ Output impedance without feedback
$Z_{\mathrm{of}}=$ Output impedance with feedback
$\mathrm{i}_{1}=$ input current
$>$ From block diagram it is clear that

$$
\mathrm{Vi}=\mathrm{Vs}-\beta \mathrm{V}_{\mathrm{o}}=\mathrm{i}_{1} \mathrm{Z}_{\mathrm{i}}
$$

Now Vs $=\left(V_{s}-\beta V_{o}\right)+\beta V_{o}=\left(v s-\beta V_{o}\right)+\beta A\left(V s-\beta V_{o}\right)=\left(V s-\beta V_{2}(1+A \beta)=i_{1} Z_{i}(1+\beta A)\right.$
Or $\mathrm{Vs} / \mathrm{i}_{1}=\mathrm{Z}_{\mathrm{i}}(1+\mathrm{mA})$
It is clear that input impedance with feedback increases by a factor $(1+\mathrm{mA})$.
Similarly, it can be derived that output impedanee, without feedback decreases by a factor ( $1+\mathrm{mA}$ ).
i.e. $\mathrm{Z}_{\mathrm{of}}=\mathrm{Z}_{\mathrm{o}} /(1+\mathrm{mA})$

## EMITTER FOLLOWER:

$>$ It is a current amplifier that has no voltage gain.
$>$ It is a negative current feedback cireuit.
$>$ It has high input impedance \& tow output impedance.
$>$ It is used for impedance matehing.
$>$ It is also known as common collector amplifier.
$>$ Circuit diagram:


## $>$ Circuit details:

It consists of transistor Q , biasing resistor R1\& R2, emitter resistor RE, input coupling capacitor $\mathrm{C}_{\mathrm{in}}$, biasing supply $+\mathrm{V}_{\mathrm{CC}}$, output coupling capacitor CC. Emitter resistance RE acts as the load \& a.c. output voltage $\mathrm{V}_{\mathrm{o}}$ is taken across $\mathrm{R}_{\mathrm{E}}$. Here biasing is provided by voltage divider method. It has no collector resistance \& no emitter bypass capacitor.
$>$ Operation:
The input voltage to be amplified is applied across the base \& emitter. The resulting ac emitter current produces an output voltage across RE. This voltage opposes the input voltage, thus providing negative feedback.

The output voltage $\mathrm{V}_{\mathrm{o}}$ is equl to input voltage i.e. output voltage follows the input voltage. Hence the name is voltage follower.

## CHARACTERISTIC OF EMITTER FOLLOWER:

$>$ No voltage gain. Practically close to one.
$>$ It has high current gain \& power gain.
$>$ It has high input impedance \& low output impedance.
$>$ Input \& output ac voltages are in phase

## CHAPTER-7 <br> MULTISTAGE AMPLIFIER

## MULTISTAGE AMPLIFIER:

$>$ When more than one stage of amplifier is connected in series then the resulting amplifier is called multistage amplifier or cascade amplifier.
> In this output of one stage acts as the input of next stage.
GAIN OF MULTISTAGE AMPLIFIER:
Suppose we consider a three stage amplifier.
$\mathrm{A}_{\mathrm{v} 1}=$ Gain of first stage
$\mathrm{A}_{\mathrm{V} 2}=$ Gain of second stage
$\mathrm{A}_{\mathrm{v} 3}=$ Gain of third stage
Then the total voltage gain, known as overall voltage gain is given by; $\mathrm{Av}=\mathrm{A}_{\mathrm{v} 1} . \mathrm{A}_{\mathrm{p}} . \mathrm{A}_{\mathrm{v}}$
FREQUENCY RESPONSE:
The graph which shows the relation between voltage gain \& frequency of an amplifier is called frequency response.
Figure shows the frequency response of a single stage amplifier.

(B)
$\mathrm{A}_{0}=$ maxium gain of anaplifier
$\mathrm{f}_{\mathrm{o}}=$ resonant frequency
$\mathrm{f}_{1}=$ lower cutoff frequency
$\mathrm{f}_{2}=$ higher ©utoff frequency
BANDWDTH:
The difference between higher cutoff frequency \& lower cutoff frequency is called bandwidth.
i.e. $B W=f_{2}-f_{1}$

Its unit is Hz .

## SPECIAL UNIT OF GAIN:

Special unit is decibel(db) or bel.One bel=10 decibel.

There are three types of gain ;
(a) Voltage gain, $\mathrm{A}_{v}=\mathrm{V}_{\mathrm{o}} / \mathrm{V}_{\mathrm{i}}=20 \log 10 \mathrm{Av}$ in db
(b) Current gain, $\mathrm{A}_{\mathrm{i}}=\mathrm{I}_{0} / \mathrm{I}_{\mathrm{i}}=20 \log 10 \mathrm{Ai}$ in db
(c) Power gain, $\mathrm{A}_{\mathrm{p}}=\mathrm{P}_{0} / \mathrm{P}_{\mathrm{i}}=10 \log 10 \mathrm{Ap}$ in db

## TYPES OF MULTISTAGE AMPLIFIER:

There are three types of multistage amplifier:
(a)RC-Coupled Amplifier
(b)Transformer Coupled Amplifier
(c)Direct coupled amplifier

## RC-COUPLED AMPLIFIER:

> It is one type of multistage amplifier, in which one stage output is coupled to the next stage by using resistor \& capacitor. Hence the name is RC-coupled.
$>$ Circuit Diagram:

$>$ Circuit detail:
Suppose we consider two stage of amplifier.

- It consists of two transistors Q1 Q 2. First stage consists of resistors $\mathrm{R}_{1}, \mathrm{R}_{2}, \mathrm{R}_{4}, \mathrm{R}_{3}$, capacitors $\mathrm{C}_{2}$, $\mathrm{C}_{3}$,transistor $\mathrm{Q}_{1}$.Second stage consists of transistor $\mathrm{Q}_{2}$, resistors $\mathrm{R}_{5}, \mathrm{R}_{6}, \mathrm{R}_{8}, \mathrm{R}_{7}$, capacitors $\mathrm{C}_{4}, \mathrm{C}_{5}$.
- $\mathrm{C}_{1}=$ Input coupling capacitor used for coupling the input signal to base of transistor $\mathrm{Q}_{1}$.It blocks dc \& allows ac only.
- Cc1=Output couplingcapacitor, which couples the amplified output of Q1 to Q2.
- $\mathrm{C}_{5}=$ output ceupling capacitor of second stage, which couples the amplified output of second stage.
- $\mathrm{R}_{1}, \mathrm{R}_{2}=\mathrm{Bi}$ Sing resistor for $\mathrm{Q}_{1}$.It provides biasing in voltage divider method.
- $\mathrm{R}_{5}, \mathrm{R}_{6} \neq$ Provides voltage divider biasing to $\mathrm{Q}_{2}$.
- $R_{3}, R_{7}=$ collector resistor of $Q_{1} \& Q_{2}$ respectively.
- $C_{2} \& C_{4}=$ Emitter bypass capacitorof $\mathrm{Q}_{1}, \mathrm{Q}_{2}$ respectively.It provides low reactance path to ac emitter current.
- $\mathrm{R}_{4}, \mathrm{R}_{8}=$ emitter resistor of $\mathrm{Q} 1, \mathrm{Q} 2$ respectively.It provides stabilisation.
- $+\mathrm{V}=$ Biasing supply.
> OPERATION:
- The a,c. signal input to be amplified is applied to the base of first transistor.The amplified output develops across $\mathrm{R}_{3}$.
- This amplified output is applied to base of transistor Q2 through coupling capacitor $\mathrm{C}_{3}$. It further amplified by $\mathrm{Q}_{2} \&$ amplified output develops across $\mathrm{R}_{7}$.
- In this way, the cascaded stages amplify the signal \& overall gain is considerably increased.


## FREQUENCY RESPONSE:

- Figure:

- The graph consists of three parts:
(a)Low frequency region
(b)High frequency Region
(c)Mid-frequency region
- Gain decreases at low \& high frequencies, remains constant at mid-frequency.
- At low frequencies: Gain decreases due to Cc \& CE. At low frequencies the reactance of Cc \& CE increases, hence very small part of the signal will pass from one stage to another. This reduces the voltage gain.
- At high frequencies, gain redqes due to parasitic/stray capacitance existing across the base emitter junction. At high frequencies reactance of Cc reduces \& acts as short path.This increases loading effect of next stage akso reduces voltage gain. The reactance of emitter base junction also reduces, which reduces B \& henee voltage gain.
- At midfrequency, as the frequency increases reactance of coupling capacitor decreases.This increases the gain.But decrease of reactance increase the loading effect \& hence gain.These two effects cancels each other. Hence gain remains constant.


## ADVANTAGES:

1-Ithasexcellent frequency response.
2-It has lower cost, since only uses capacitors \& resistors which are cheap.
3-The circuit is very compact \& light in weight.

## DISADVANTAGES:

1-It has low voltage \& power gain.

2-They have the tendency to become noisy with age.
3-It has poor impedance matching.

## APPLICATION

Widely used as voltage amplifier.

## TRANSFORMER COUPLED AMPLIFIER:

$>$ The multistage amplifier in which one stage is connected to next stage using a coupling transformer is called transformer coupled amplifier.
> Circuit Diagram:

$\mathrm{R}_{1}, \mathrm{R}_{2}=$ biasing resistor for both stages in voltage divider rule.
$\mathrm{R}_{\mathrm{E}}=$ Emitter resistor of $\mathrm{Q} 1 \& \mathrm{Q} 2$ \& provides stabilisation.
$\mathrm{C}_{\mathrm{E}}=$ Emitter bypass capacitor for $\mathrm{Q} 1 \& \mathrm{Q} 2$ respeetively.
T1,T2=Coupling transformers.It increases the effective load resistance of each stage, hence increase thevoltage \& power gain.It also provides good impedance matching.
$\mathrm{C}_{\mathrm{in}}=$ input coupling capacitor, which couples the input to $\mathrm{Q}_{1}$.
> OPERATION:

- The input signal to be amplified is applied to the base of $\mathrm{Q}_{1} \&$ amplified output develops across the primary of T1.It transfers to the secondary \& applied to base of transistor $\mathrm{Q}_{2}$ i.e. to second stage for further amplification.
- Due to transforner coupling the effective load resistance of each stage increases. This increases the voltage gain\& power gain.
- It provides good impedance matching between two stages of amplifier.
- It mostly used for power amplification.
- Transformer coupling is used in case of small load resistance.


## FREQUENCY RESPONSE:



It is clear from the graph that frequency response is poor as compared to RC-coupled amplifier. It provides constant gain only over a small range of frequencies. Gain decreases at low \& high frequencies. At low frequencies, reactance of primary winding decreases \& this decreases the gain, Athigh frequencies, capacitance between turns of windings act as a bypass capacitor to reducethe output voltage \& hence gain.

## ADVANTAGES:

$>$ No signal power is lost in the collector or base resistors.
$>$ Provides good impedance matching.
> Provides higher power gain \& voltage gain.

## DISADVANTAGES:

$>$ It has poor frequency response.
$>$ Coupling transformers are bulky \& fairly expensive at autdio range.
$>t$ has frequency distortion. Low frequency signals are ress amplified as compared to high frequency signals.

## DIRECT COUPLED AMPLIFIER:

$>$ The multistage amplifier in which one stage is connected to next stage directly without using any coupling element is called direct coupled amplifier.
> Circuit diagram:


## > Circuit Detail:

- Suppose we consider a three stage amplifier.It uses complementary transistors i. e. if first stage uses npn, the second stage uses pnp transistor \& so on.
- It consists of three transistors T1, T2, T3,three identical collector resistors Rc for each stage.
$>$ Operation:

The input signal to be amplified is applied to base of T1 \& the amplified output from collector of T1 is applied to base of T2 for further amplification \& so on.

- It is suitable for amplifying very low frequencies i.e. $<10 \mathrm{~Hz}$.
- It amplifies photo-electric current, thermocouple current etc.



## REFERENCES

1- Principle of Electronics- By V.K. Meheta
2- Electronic Devices and Circuits- By David A. BELL
3- Basic Electronics - By J.B. Gupta
4- Google site for circuits.


[^0]:    *The process of applying external voltage across the pn-junction is called biasing.
    *Types of biasing :

[^1]:    > Cincuit diagram:

