

# LESSON PLAN

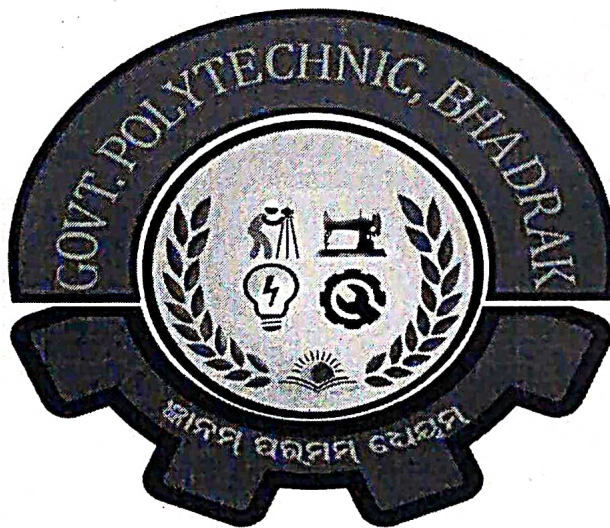
**SUB: DIGITAL ELECTRONICS & MICROPROCESSOR LAB**

**BRANCH:- ELECTRICAL ENGG.**

**SEMESTER: 5<sup>th</sup>**

**SESSION:2024-2025**

**NAME OF FACULTY: TAPAN KUMAR DAS**



**GOVERNMENT POLYTECHNIC,  
BHADRAK**

Hod, Electrical  
HOD (ELECT.)  
G.P. BHADRAK

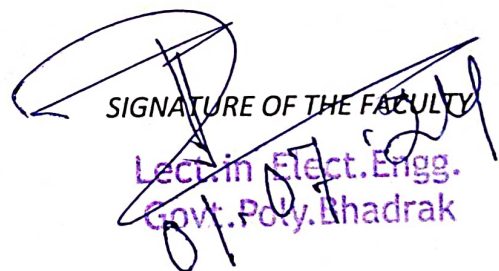
Academic Co-ordinator  
Academic Co-ordinator

Principal  
Govt. Polytechnic, Bhadrak  
Principal  
Govt. Polytechnic  
Bhadrak

<b>DISCIPLINE</b> <b>ELECTRICAL</b> <b>ENGG.</b>	<b>SEMESTER</b> <b>5<sup>TH</sup></b>	<b>NAME OF THE</b> <b>TEACHING FACULTY</b> <b>TAPAN KUMAR DAS (Lect. in Elect. Engg.)</b>
<b>SUBJECT</b> <b>DIGITAL</b> <b>ELECTRONICS &amp;</b> <b>MICROPROCESSOR</b> <b>LAB</b>	<b>NO. OF DAYS/WEEK</b> <b>CLASS ALLOTTED – 45</b> <b>(3P/week)</b>	<b>SEMESTER</b> <b>FROM DATE</b> <b>01.07.2024 to</b> <b>08.11.2024</b>
<b>WEEK</b>	<b>CLASS DAY</b>	<b>PRACTICAL TOPICS</b>
1st	01	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates.
	02	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates.
2nd	01	Implement various gates by using universal properties of NAND & NOR gates and verify truth table
	02	Implement various gates by using universal properties of NAND & NOR gates and verify truth table
3rd	01	Implement half adder and Full adder using logic gates
	02	Implement half adder and Full adder using logic gates
4th	01	Implement half subtractor and Full subtractor using logic gates
	02	Implement half subtractor and Full subtractor using logic gates
5TH	01	Implement a 4-bit Binary to Gray code converter
	02	Implement a 4-bit Binary to Gray code converter
6TH	01	Implement a Single bit digital comparator

	02	Implement a Single bit digital comparator
7 <sup>TH</sup>	01	Study Multiplexer and demultiplexer
	02	Study Multiplexer and demultiplexer
8 <sup>TH</sup>	01	Study of flip-flops. i) S-R flip flop ii) J-K flip flop iii) flip flop iv) T flip flop
	02	Study of flip-flops. i) S-R flip flop ii) J-K flip flop iii) flip flop iv) T flip flop
9 <sup>TH</sup>	01	Realize a 4-bit asynchronous UP/Down counter with a control for up/down counting
	02	Realize a 4-bit asynchronous UP/Down counter with a control for up/down counting
10 <sup>TH</sup>	01	Implement Mode-10 asynchronous counters
	02	Implement Mode-10 asynchronous counters
11 <sup>TH</sup>	01	General Programming using 8085A development board a. 1'S Complement. b. 2'S Complement
	02	General Programming using 8085A development board a. 1'S Complement. b. 2'S Complement
12 <sup>TH</sup>	01	General Programming using 8085A development board Addition of 8-bit number. b. Subtraction of 8-bit number resulting 8/16 bit number
	02	General Programming using 8085A development board Addition of 8-bit number. b. Subtraction of 8-bit number resulting 8/16 bit number
13 <sup>TH</sup>	01	Execute the different Ladder Diagram General Programming using 8085A development

		board a. Decimal Addition 8-bit number. b. Decimal Subtraction 8-bit number s
	02	Execute the different Ladder Diagram General Programming using 8085A development board a. Decimal Addition 8-bit number. b. Decimal Subtraction 8-bit number s
14 <sup>TH</sup>	01	Interfacing using 8085 Traffic light control using 8255.
	02	Interfacing using 8085 Traffic light control using 8255.
15 <sup>TH</sup>	01	Interfacing using 8085 . Generation of square wave using 8255
	02	Interfacing using 8085 Generation of square wave using 8255

  
 SIGNATURE OF THE FACULTY  
 Lect.in Elect. Engg.  
 Govt. Poly. Bhadrak