

# LESSON PLAN

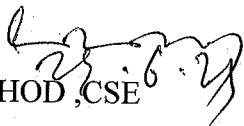
**SUB: COMPUTER SYSTEM ARCHITECTURE, (TH-1)**  
**BRANCH:- COMPUTER SCIENCE & ENGINEERING**  
**SEMESTER:3<sup>RD</sup>**

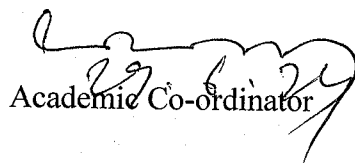
**NAME OF FACULTY: LAXMIDHAR SETHY(SR.LECT.IN CSE)**

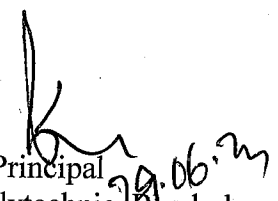


## GOVERNMENT POLYTECHNIC, BHADRAK

SESSION ~: 2024-25

  
HOD, CSE

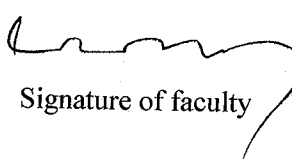
  
Academic Co-ordinator

  
Principal  
Govt. Polytechnic, Bhadrak  
Principal  
Govt. Polytechnic  
Bhadrak

|  |   |   |
|--|---|---|
| <b>Discipline:</b> Computer Science & Engineering    | <b>Semester:</b> 3 <sup>rd</sup> , W/2024 | <b>Name of the faculty:</b> Laxmidhar Sethy<br><b>Email:</b> <a href="mailto:ldsathy@gmail.com">ldsathy@gmail.com</a> |
| <b>Subject:</b> Computer System Architecture, (Th-1) | <b>No. of Days/week:</b> 04               | <b>StartDate:</b> 01/07/2024<br><b>EndDate:</b> 08/11/2024  |

| Week             | Class Day       | Theory Topics   |
|------------------|-----------------|---|
| 1 <sup>st</sup>  | 1 <sup>st</sup> | <b>1.IntroductiontoBasicstructureofcomputerhardware</b>       |
|                  | 2 <sup>nd</sup> | Introduction of computer                                      |
|                  | 3 <sup>rd</sup> | Basic Structure of computer                                   |
|                  | 4 <sup>th</sup> | Computer hardware   |
| 2 <sup>nd</sup>  | 1 <sup>st</sup> | Functional Units  |
|                  | 2 <sup>nd</sup> | Computer components   |
|                  | 3 <sup>rd</sup> | Performance measures  |
|                  | 4 <sup>th</sup> | Memory addressing & Operations                                |
| 3 <sup>rd</sup>  | 1 <sup>st</sup> | Revision  |
|                  | 2 <sup>nd</sup> | <b>2.IntroductiontoInstructions&amp;instructionSequencing</b> |
|                  | 3 <sup>rd</sup> | Fundamentals to instructions                                  |
|                  | 4 <sup>th</sup> | Operands  |
| 4 <sup>th</sup>  | 1 <sup>st</sup> | Op Codes  |
|                  | 2 <sup>nd</sup> | Instruction formats   |
|                  | 3 <sup>rd</sup> | Addressing Modes  |
|                  | 4 <sup>th</sup> | Continuing addressing modes                                   |
| 5 <sup>th</sup>  | 1 <sup>st</sup> | Revision  |
|                  | 2 <sup>nd</sup> | Question answer discussion                                    |
|                  | 3 <sup>rd</sup> | <b>3.IntroductiontoProcessorSystem</b>                        |
|                  | 4 <sup>th</sup> | Register Files  |
| 6 <sup>th</sup>  | 1 <sup>st</sup> | Complete instruction execution                                |
|                  | 2 <sup>nd</sup> | Hardware control  |
|                  | 3 <sup>rd</sup> | Micro program control   |
|                  | 4 <sup>th</sup> | Revision  |
| 7 <sup>th</sup>  | 1 <sup>st</sup> | Quiz-1  |
|                  | 2 <sup>nd</sup> | <b>4.Introduction to Memory System</b>                        |
|                  | 3 <sup>rd</sup> | Memory characteristics  |
|                  | 4 <sup>th</sup> | Memory hierarchy  |
| 8 <sup>th</sup>  | 1 <sup>st</sup> | RAM and ROM organization                                      |
|                  | 2 <sup>nd</sup> | Continuing about RAM and ROM organization                     |
|                  | 3 <sup>rd</sup> | Interleaved Memory  |
|                  | 4 <sup>th</sup> | Cache memory  |
| 9 <sup>th</sup>  | 1 <sup>st</sup> | Virtual memory  |
|                  | 2 <sup>nd</sup> | Revision  |
|                  | 3 <sup>rd</sup> | Question answer discussion                                    |
|                  | 4 <sup>th</sup> | <b>5.IntroductiontoInput-OutputSystem</b>                     |
| 10 <sup>th</sup> | 1 <sup>st</sup> | Input-Output Interface  |

|                  |                 |   |
|------------------|-----------------|---|
|                  | 2 <sup>nd</sup> | Modes of Data transfer  |
|                  | 3 <sup>rd</sup> | Programmed I/O Transfer                                       |
|                  | 4 <sup>th</sup> | Interrupt driven I/O  |
| 11 <sup>th</sup> | 1 <sup>st</sup> | DMA   |
|                  | 2 <sup>nd</sup> | I/O Processor   |
|                  | 3 <sup>rd</sup> | Continuing I/O Processor                                      |
|                  | 4 <sup>th</sup> | Revision  |
| 12 <sup>th</sup> | 1 <sup>st</sup> | Question answer discussion                                    |
|                  | 2 <sup>nd</sup> | <b>6.Introduction to I/O Interface &amp; Bus architecture</b> |
|                  | 3 <sup>rd</sup> | Bus and System Bus  |
|                  | 4 <sup>th</sup> | Types of System Bus   |
| 13 <sup>th</sup> | 1 <sup>st</sup> | Bus Structure   |
|                  | 2 <sup>nd</sup> | Basic Parameters of Bus design                                |
|                  | 3 <sup>rd</sup> | SCSI  |
|                  | 4 <sup>th</sup> | USB   |
| 14 <sup>th</sup> | 1 <sup>st</sup> | Revision  |
|                  | 2 <sup>nd</sup> | Quiz-2  |
|                  | 3 <sup>rd</sup> | <b>7.Introduction to Parallel Processing</b>                  |
|                  | 4 <sup>th</sup> | Parallel Processing   |
| 15 <sup>th</sup> | 1 <sup>st</sup> | Linear Pipeline   |
|                  | 2 <sup>nd</sup> | Multiprocessor  |
|                  | 3 <sup>rd</sup> | Flynn"s Classification  |
|                  | 4 <sup>th</sup> | Revision  |

  
Signature of faculty