DISCIPLINE ***ELECTRICAL***	SEMESTER ***5TH***	NAME OF THE TEACHING FACULTY UMESH KUMAR DALAI
SUBJECT ***DIGITAL ELECTRONICS & MICROPROCESSOR***	NO. OF DAYS/WEEK CLASS ALLOTTED - 75	SEMESTER FROM DATE 14.07.2025 to 15.11.2025
WEEK	CLASS DAY	THEORY TOPICS
1ST	01	BASICS OF DIGITAL ELECTRONICS Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	02	Binary addition, subtraction, Multiplication and Division.
	03	1‘s complement and 2‘s complement numbers for a binary number.
	04	Subtraction of binary numbers in 2‘s complement method.
	05	Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
2ND	06	Importance of parity Bit.
	07	Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	08	Realize AND, OR, NOT operations using NAND gates.
	09	Realize AND, OR, NOT operations using NOR gates.
	10	Different postulates and De-Morgan‘s theorems in Boolean algebra.
3RD	11	Use Of Boolean Algebra For Simplification Of Logic Expression.
	12	Karnaugh Map For 2 &3Variable
	13	Karnaugh Map For 4 Variable.
	14	Simplification Of SOP And POS Logic Expression Using K-Map.
	15	Revision of chapter 1.
4TH	16	Give the concept of combinational logic circuits.
	17	Half adder circuit and verify its functionality using truth table.
	18	Realize a Half-adder using NAND gates only and NOR gates only.
	19	Full adder circuit and explain its operation with truth table.
	20	Realize full-adder using two Half-adders and an OR – gate and write truth table.
5TH	21	Full subtractor circuit and explain its operation with truth table.
	22	Operation of 4 X 1 Multiplexers.
	23	1 X 4 demultiplexer.
	24	Working of Binary-Decimal Encoder
	25	3 X 8 Decoder
6TH	26	Working of Two bit magnitude comparator.
	27	Revision of chapter 2.
	28	Revision of chapter 2.
	29	Give the idea of Sequential logic circuits
	30	State the necessity of clock and give the concept of level clocking and edge triggering.
7TH	31	Clocked SR flip flop with pre-set and clear inputs.
	32	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table.
	33	Concept of race around condition and study of master slave JK flip flop.

	34	Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	35	Applications of flip flops.
8TH	36	Define modulus of a counter.
	37	4-bit asynchronous counter and its timing diagram.
	38	Asynchronous decade counter.
	39	4-bit synchronous counter.
	40	Distinguish between synchronous and asynchronous counters
9TH	41	State the need for a Register and list the four types of registers.
	42	Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
	43	Revision of chapter 3.
	44	Revision of chapter 3.
	45	Introduction to Microprocessors, Microcomputers.
10TH	46	Architecture of Intel 8085A Microprocessor and description of each block.
	47	Pin diagram and description.
	48	Stack, Stack pointer & stack top.
	49	Interrupts.
	50	Opcode & Operand.
11TH	51	Differentiate between one byte, two byte & three byte instruction with example.
	52	Instruction set of 8085 example.
	53	Instruction set of 8085 example.
	54	Instruction set of 8085 example.
	55	Addressing mode.
12TH	56	Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	57	Timing Diagram for memory read, memory write, I/O read, I/O write
	58	Timing Diagram for memory read, memory write, I/O read, I/O write
	59	Timing Diagram for 8085 instruction.
	60	Counter and time delay.
13TH	61	Simple assembly language programming of 8085.
	62	Revision of chapter 4.
	63	Revision of chapter 4.
	64	Basic Interfacing Concepts.
	65	Memory mapping & I/O mapping.
14TH	66	Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	67	Application using 8255: Seven segment LED display.
	68	Square wave generator.
	69	Traffic light Controller.
	70	Revision of chapter 5.
15TH	71	Revision of chapter 1.
	72	Revision of chapter 2.
	73	Revision of chapter 3.
	74	Revision of chapter 4.
	75	Revision of chapter 5.