LESSON PLAN

SUB: MICROPROESSOR & MICROCONTROLLER
BRANCH:- COMPUTER SCIENCE& ENGG.
SEMESTER:4th
NAME OF FACULTY: LAXMIDHAR SETHY (SR, LECT, in CSE)

GOVERNMENT POLYTECHNIC, BHADRAK

SESSION: 2025-26

Hod ,CSE 18.12.25

Academic Co-ordinator 18.12.25
Academic Co-ordinator

Principal
Govt. Polytechnic, Bhadrak

DEPARTMENT OF Computer Science & Engg,,

Discipline: Computer Science and Engineering	Semester: 4th Summer/2025	Name of the Faculty: Laxmidhara sethy(Sr. lect,in cse) Email ID:ldsethy@gmail.com
Subject: MICROPROCESSOR AND MICROCONTROLLER TH.3	No. of Days/week: 04 Period:03	Start Date:22/12/2025 End Date:18/04/2026

Week	Class Day	Theory Topic
1st	1st	Discussion of microprocessor and its application
	2nd	Distinguish between microprocessor and microcomputer
	3rd	Discussion of Architecture of processor and Bus system in processor
	4th	Pin configuration of Intel 8085 microprocessor
	5th	Architecture of Intel 8085 processor
2nd	1st	Revising the taught portions
	2nd	Doubt clearance
	3rd	Pin configuration of Intel 8085 microprocessor
	4th	Architecture of Intel 8085 processor
	5th	Architecture of Intel 8085 processor
3rd	1st	Registers of Intel 8085. Distinguish between SPR and GPR
	2nd	Stack, stack pointer and stack top
	3rd	Addressing modes in Intel 8085
	4th	Addressing modes in Intel 8085
	5th	Architecture of Intel 8085
4th	1st	Types of instruction
	2nd	Types of instruction
	3rd	Simple programming examples
	4th	Basic assembler Directives

	5th	Programming on logic operations
5th	1st	Programming on logic operations
	2nd	Programming on Delay
	3rd	Programming on Delay
	4th	Programming on looping, counting, Indexing (JMP and CALL)
	5th	Compare between two numbers, Arrray Handling, code conversion
6th	1st	T-state, Fetch cycle, Machine cycle and Instruction cycle
	2nd	T-state, Fetch cycle, Machine cycle and Instruction cycle
	3rd	Differentiate between Instruction cycle, machine cycle and T state
	4th	Timing diagram of MOV,DCR,MVI,LDA,DCX
	5th	Timing diagram of MOV,DCR,MVI,LDA,DCX
7th	1st	Timing diagram of MOV,DCR,MVI,LDA,DCX
	2nd	Timing diagram of MOV,DCR,MVI,LDA,DCX
	3rd	Revision of Timing diagram Doubt clearance
	4th	Pin configuration of Intel 8255 and discussion of interfacing
	5th	Pin configuration of Intel 8255 and discussion of interfacing
8th	1st	Memory mapping and IO mapping
	2nd	Memory interfacing with RAM and EPROM
	3rd	8257 DMA controller
	4th	Traffic light controlling, stepper motor control
	5th	Traffic light controlling, stepper motor control
9th	1st	ADC and DAC interfacing
	2nd	Internal architecture of Intel 8086, maximum and minimum mode
	3rd	Internal architecture of Intel 8086, maximum and minimum mode
	4th	Assignment
	5th	Checking of assignment
10th	1st	Class test
	2nd	Internal ready revision
	3rd	Pin details of 8086
	4th	Pin details of 8086
	5th	Pin details of 8086
11th	1st	Addressing modes of 8086
	2nd	Instruction set of 8086

	3rd	Instruction set of 8086
	4th	Simple programming
	5th	Simple programming
12th	1st	Addressing modes of Intel 8086
	2nd	Distinguish between Microprocessor & Microcontroller
	3rd	8 bits & 16-bit microcontroller
	4th	CISC & RISC processor
	5th	Architecture of 8051 Microcontroller
13th	1st	Signal Description of 8051 Microcontrollers
	2nd	Signal Description of 8051 Microcontrollers
	3rd	Memory Organisation-RAM structure, SFR
	4th	Registers, timers, interrupts of 8051 Microcontrollers
	5th	Registers, timers, interrupts of 8051 Microcontrollers
14th	1st	Addressing modes of 8051
	2nd	Simple 8051 Assembly Language Programming Arithmetic & Logic Instructions, JUMP, LOOP, CALL Instructions, I/O Port Programming
	3rd	Interrupts, Timer & Counters, Serial Communication
	4th	Microcontroller interrupts and interfacing with 8255
	5th	Microcontroller interrupts and interfacing with 8255
15th	1st	Final revision, previous year questions discussion.
	2nd	Final revision, previous year questions discussion.
	3rd	Practice test
	4th	Practice test
	5th	Practice Test

18/12/23

Signature of faculty