LESSON PLAN

SUB:- DIGITAL ELECTRONICS AND MICROPROCESSOR

DEPT. OF ELECT. ENGG. GOVT. POLY. BHADRAK ESTD-2017

BRANCH:- ELECTRICAL ENGG.

SEMESTER:5th

NAME OF FACULTY: - SUSHANT KUMAR MOHANTY

GOVERNMENT POLYTECHNIC, BHADRAK

SESSION:2026-27

HOD Electrical
HOD (ELECT.)
G.P.BHADRAK

Academic Co-ordinator
Academic Co-ordinator

Principal
Govt. Polytechnic Bhadrak
Principal
Govt.Polytechnic
Bhadrak

LESSON PLAN

DIGITAL ELECTRONICS AND MICROPROCESSOR

Course Code- EEPC301 TH3- 5th semester

NAME: SUSHANT KUMAR MOHANTY . LECT: ETC , W.E.F:01.07.2026 TO 05.11.2026

SUB: DIGITAL ELECTRONICS AND MICROPROCESSOR

BRANCH: ELECTRICAL ENGG.

NO OF PERIODS /WEEK: 3	CLASS NO & TOPICS TO BE COVERED	REMARK
WEEK-1	**Digital Fundamentals** Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates and truth tables, Universal gates, .	
WEEK-2	Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and QuineMcCluskey method of minimization	
WEEK-3	**Combinational & Synchronous Sequential Circuits** Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder	
WEEK-4	Multiplexer, Demultiplexers, Decoders, and Priority Encoder.	
WEEK-5	Flip flops – SR, JK, T, D, design of clocked sequential circuits – Design of Counters- Shift registers, Universal Shift Register.	
WEEK-6	**Asynchronous Sequential Circuits And Memory Devices** Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Pulse mode sequential circuits,	
WEEK-7	Design of Hazard free circuits. Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM, RAM – Static and dynamic RAM –	
WEEK-8	Programmable Logic Devices – Programmable Logic Array (PLA) – Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA).	
WEEK-9	**8085 Processor** Hardware Architecture, pin diagram	
WEEK-10	Functional Building Blocks of Processor – Memory organization – I/O ports and data transfer concepts	
WEEK-11	Timing Diagram – Interrupts.	

WEEK-12	**Programming Processor** Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions – Programming: Loop structure with counting & Indexing – Look up table – Subroutine instructions – stack -8255 architecture and operating modes	
WEEK-13	**Programming Processor** Instruction – format and addressing modes – Assembly language format – Data transfer, data manipulation & control instructions	
WEEK-14	Programming: Loop structure with counting & Indexing	
WEEK-15	Look up table – Subroutine instructions – stack -8255 architecture and operating modes	

Sushant 30/06/26

Signature of Faculty